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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	**09/811,647**
Applicant	:	**Vickram R. Vathulya**
Title of Invention	:	**CIRCUIT AND METHOD FOR INPUT SIDE IMPEDANCE MATCHING OF A POWER AMPLIFIER IN AN ELECTRONIC DEVICE**
Date Filed	:	**March 19, 2001**
T.C./AU	:	**2817**
Examiner	:	**JONES, Stephen E.**
Docket No.	:	**US 010082**

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

REMARKS

This is responsive to the Office Action dated May 21, 2003 in which the Examiner rejects all the pending claims 1- 20 as either being anticipated by Utsu (US Patent No. 5,343,172) under 35 USC §102(b) or as being obvious over Utsu, or further in view of Kleveland (WO 98/47190) under 35 USC §103(a). Applicant respectfully traverses the rejections of the Examiner, as explained in detail below.

In the current Office Action the Examiner rejects all the pending claims 1-20 simply based upon "the reasons of record." Applicant has reviewed the previous Office Actions and Responses to find "the reasons of record." Applicant finds that only in the first Office Action dated July 18, 2002 did the Examiner detail why the present invention was anticipated by Utsu. In particular, in that

Office Action of July 18, 2002, the Examiner asserted that the impedance transformer network in claim 1 was met by the parallel variable reactance circuit 14 in Utsu. In his response, applicant amended claim 1 to define the impedance transformer network as one to synthesize the predetermined impedance (of the source signal) at an input of the power amplifier, so as to distinguish it from the reactance circuit 14 in Utsu, which does NOT synthesize the predetermined impedance at the input of the power amplifier.

In the final Office Action dated January 7, 2003, the Examiner held his opinion that the parallel reactance circuit 14 can be read as the impedance transformer network in claim 1 on an assertion that the series capacitor 12, which constitutes the impedance matching network together with the parallel reactance circuit 14, was not an important part of the impedance matching network in Utsu. The current office action is a result of a further examination on that RCE/Response.

Thus, it appears in the current Office Action that the Examiner holds that the parallel reactance circuit 14 in Utsu is to be read as the impedance transformer network in claim 1 of the present invention. The applicant respectfully disagrees for reasons detailed below.

First, it is clearly defined in claim 1 that the impedance transformer network is a network to synthesize the predetermined impedance (of the source signal) at an input of the power amplifier. The applicant respectfully disagrees with the conclusion of the Examiner that any component element in the impedance matching circuit may be read as the circuit itself only because "without it (reactance circuit 14), the proper impedance would not result" (see page 3 of Office Action dated January 7, 2003). The applicant would like to emphasize that the impedance synthesized by the network is the predetermined impedance of the source signal, not a portion of the predetermined impedance. In other words, a portion of the predetermined impedance is NOT the predetermined impedance. For example, a value of 10 can be a sum result of 4 and 6, but neither 4 or 6 can be deemed as 10. Following such reasoning, any element or sub-circuit in the impedance matching circuit, such as any

resistor, conductor or capacitor, can be read as the circuit itself. Applicant respectfully submits that this is unreasonable.

The applicant believes that the impedance transformer network in claim 1 cannot be read into the parallel variable reactance circuit 14, but is to be read as the matching impedance circuit which includes the parallel reactance circuit 14 **and** the series reactance element 12. In other words, the impedance transformer network in claim 1 is the combination of the parallel reactance circuit 14 **and** the series reactance element 12.

Moreover, the applicant respectfully disagrees with the assertion of the Examiner that the impedance matching circuit in Utsu, which, as explained above, includes both the parallel reactance circuit 14 and the series reactance element 12, can be deemed as "in parallel" with the source because a part (apparently the parallel reactance circuit 14) of the matching circuit is in parallel with the source. Such assertion lacks any support and the applicant believes it is totally wrong. As is common knowledge in the electrical field, the impedance matching circuit as a whole, which is a combination of a parallel portion 14 and a series portion 12, is neither in parallel, nor in series, with the source.

Summing up the above, the applicant believes: 1) the parallel reactance circuit 14 in Utsu is not the impedance transformer network in claim 1 because it does NOT synthesize the predetermined impedance of the source signal at the input of the amplifier; and 2) if the impedance matching circuit in Utsu is read as the impedance transformer network in claim 1, it is NOT in parallel with the source, even though it includes a parallel reactance circuit.

Therefore, the applicant believes that independent claim 1, with the distinguishing features that the circuit comprises an impedance transformer network to synthesize the predetermined impedance at the input of the power amplifier **AND** the impedance transformer network is in parallel with the source, is not anticipated by the Utsu patent under 35 USC §102(b). The above distinguishing features cannot be found in Kleveland (WO 98/47190) either. Therefore, claim 1 is

believed patentable. Similarly, claims 10 and 15, both including the above distinguishing features, are also believed patentable for the same explanations as to claim 1.

At least for the same reasons, the applicant believes dependent claims 2-9, 11-14 and 16-20 are also patentable, as each of them includes all the limitations of one of the dependent claims 1, 10 and 15.

The applicant therefore respectfully requests reconsideration and allowance in view of the above remarks. The Examiner is authorized to deduct additional fees believed due from our Deposit Account No. 11-0223.

Respectfully submitted,

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Dated: August 8, 2003

Jeffrey I. Kaplan
(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on August 8, 2003.

Dated August 8, 2003 Signed Paula M. Halsey Print Name Paula M. Halsey

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